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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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7590

08/27/2003

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EXAMINER

WARREN, MATTHEW E

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 08/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/109,261

Applicant(s)

BAI

Examiner

Matthew E. Warren

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 June 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 8-10,12-17 and 19-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 8-10,12-17,19-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Supplemental Amendment filed on June 10, 2003.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 8-10, 14-17, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata et al. (US 4,015,281) and Momose et al. (US 5,990,516).

Nagata discloses (col. 3, line 45 – col. 4, line 67) a transistor device having a gate electrode overlying a gate dielectric formed directly on a semiconductor substrate. The dielectric (col. 4, lines 34-49) comprises a first dielectric having a first dielectric constant and a second dielectric having a second dielectric constant different from the first dielectric constant. The first and second dielectrics are scalable for a set of feature size technologies, wherein the first and second dielectric thickness are determined by the formula as recited in claims 8 and 15 (see the expanded formula in col. 4, lines 39-44). The second dielectric (Al_2O_3) has a greater dielectric constant than the first dielectric (SiO_2) (col. 4, lines 45-49). A third dielectric ($\text{SiO}_2\text{-P}_2\text{O}_5$), having a third dielectric constant may also be used in the composite dielectric layer (col. 4, lines 50-56). Nagata et al. shows all of the elements of the claims except the set of feature size technologies defined by a gate length in the range of 25-150 nm. Momose et al.

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discloses (col. 16, 28-48 and col. 16, line 66-col. 17, line 32) a semiconductor device having double layer gate dielectric in which the feature size technology has a gate length of 150 nm (or 0.15 μm) to form a high performance semiconductor having low power consumption. Momose et al. further discloses (col. 15, lines 13-31) that the gate length can be decreased even more to improve the current drive capability. The gate in one embodiment had a length of 40 nm (0.04 μm). Momose et al. also discloses (col. 2, lines 52-58) a semiconductor device in which the gate dielectric is less than 1/3 the gate length. The thin gate dielectric improves hot carrier reliability and ultimately the operating characteristics. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the multi-layer gate dielectric of Nagata for a feature size technology with a desired gate length as taught by Momose to form a high performance transistor having low power consumption.

Claims 12, 13, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata et al. (US 4,015,281) and Momose et al. (US 5,990,516) as applied to claims 8 and 15 above, and further in view of Gardner et al. (US 6,005,274).

Nagata et al. in view of Momose et al. shows all of the elements of the claims except the materials of first and second dielectric layers. Gardner shows (fig. 3D) a semiconductor device having a multi-layered gate dielectric formed directly on the substrate. The first dielectric layer (303) of the gate dielectric is formed on the substrate. The first dielectric layer is silicon nitride (col. 5, lines 25-44). The second dielectric layer of the gate dielectric is a high dielectric constant material (305) of BST (col. 3, lines 15-

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43) and is formed on the first dielectric layer. The dielectric constant of the first dielectric layer (SiN) is less than the dielectric constant of the second dielectric layer (BST). A gate electrode (307a) is formed on the multi-layered gate dielectric. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the gate dielectric Nagata and Momose by using BST for the composite dielectric layer as taught by Gardner to provide suitable gate insulation.

Response to Arguments

Applicant's arguments filed with respect to claims 8 and 15 have been fully considered but they are not persuasive. The applicant primarily asserts the prior art references do not show all of the elements of the claims, specifically that the MOSFET of Momose is not scalable for a gate length in the range of 25-70nm. The examiner believes that the cited references show all of the elements of the claims and that Momose in particular cures the deficiencies of Nagata et al. by disclosing the amended limitations of the claims. It is the examiner's view that the applicant is attempting to circumvent Momose by narrowing the gate length requirements of the invention from the range of 25-150 nm down to a range of 25-70 nm. The applicant's specification does not disclose the criticality of the narrow range so it is not understood why such a limitation is distinguishable over the cited art. Even if such a range were critical to the invention, Momose, who deals with the scalability of gate dielectrics, discloses that MOSFETS have been achieved having a gate length of at least 40 nm (0.04 μm) (see col. 15, lines 13-31). Therefore, Momose cures the deficiencies of Nagata by disclosing the

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scalability of a feature size technology defined by a gate having the applicant's desired range. The combined references show all of the elements of the claims and this action is made final.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (703) 305-0760. The examiner can normally be reached on Mon-Thurs, and alternating Fri, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

MEW
MEW
August 22, 2003



ALLAN R. WILSON
PRIMARY EXAMINER